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EECS 301

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Lab 1 report

**Design Questions**

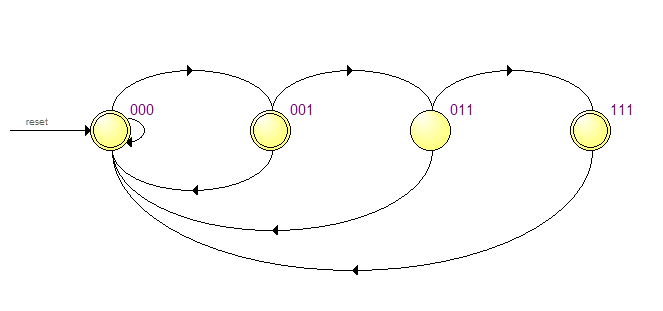
1. For the turn module, there are 7 states (3 active turning sequences for each side and idle state for both idle and error.

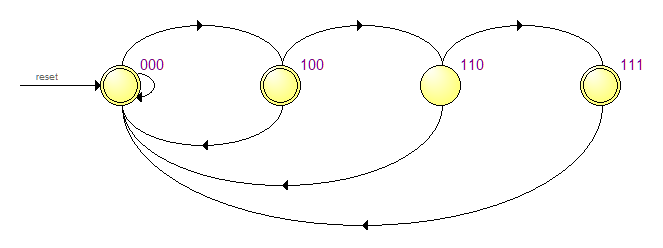
For the brake module, there are 3 states (non-braking state that bypasses turning, braking state and braking delaying state).

1. The ~3Hz clock used 24 bits, as (50\*106)/(224) ~ 3.
2. The buttons (KEY) are active-low
3. The state machine diagram would show the module if the Verilog state machine syntax is implemented correctly in Quartus

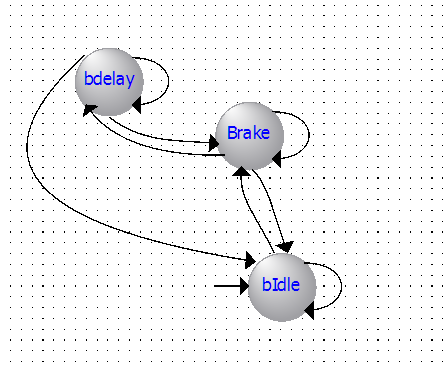
**Report Requirement**

Two parts for left and right turn state diagrams:

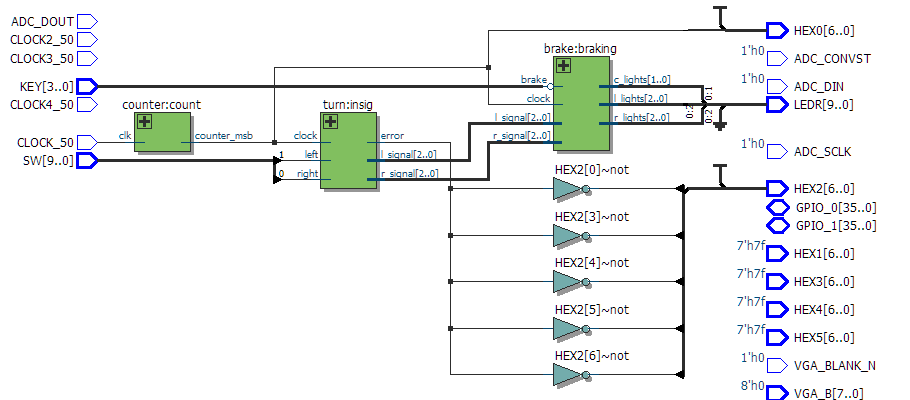




Braking module:

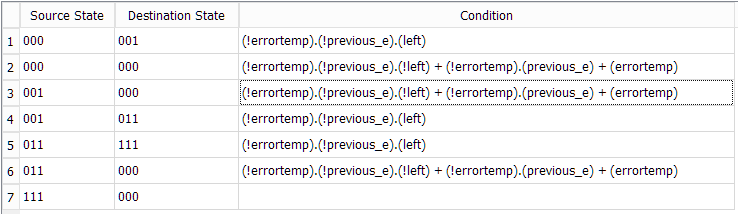


Block diagram of the hierarchy:

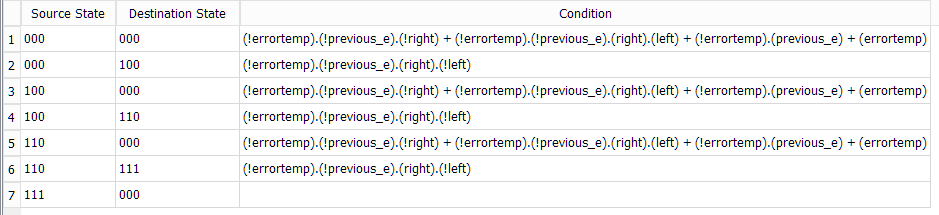


State assignments of Quartus

Turning left:



Turning right:



Quartus does not recognize the brake state machine (possibly due to the delay handling that used a integer sum).

Summary of collaboration:

We used github setup by jem177 to exchange progress and update code, while this report is written by jxw585.